What is claimed is:

1. A microelectronic device comprising:

a die fixed within a package core;

a metallization layer built up upon said die and said package core; and

a grid array interposer unit having a first surface laminated to said metallization layer, said grid array interposer unit having an array of electrical contacts on a second surface thereof for connection to an external circuit board.

2. The microelectronic device claimed in claim 1, wherein:

said metallization layer includes a first metallization portion located over said die and a second metallization portion located over said package core

3. The microelectronic device claimed in claim 1, comprising:

at least one de-coupling capacitor connected to said second surface of said grid array interposer unit to provide de-coupling for circuitry within said die.

4. The microelectronic device claimed in claim 3, wherein:

said grid array interposer unit has a thickness between said first and second surfaces that is no greater than 0.5 millimeters.

5. The microelectronic device claimed in claim 1, wherein:

said grid array interposer unit includes an opening that exposes a first portion of said metallization layer, said microelectronic device further comprising at least one de-coupling capacitor connected to said first portion of said metallization layer to provide de-coupling for circuitry within said die.

6. The microelectronic device claimed in claim 1, wherein:

said die is fixed within said package core using an encapsulation material.

7. The microelectronic device claimed in claim 1, wherein:

said package core is formed from a dielectric board material having a metallic cladding on at least one surface thereof.

8. The microelectronic device claimed in claim 7, wherein:

said metallic cladding is conductively coupled to ground during operation of said device to provide a ground plane for at least one transmission structure within said metallization layer.

9. The microelectronic device claimed in claim 7, wherein:

said metallic cladding is conductively coupled to a power source during device operation to form a power plane.

10. The microelectronic device claimed in claim 7, wherein:

said metallization layer includes at least one ground pad that is conductively coupled to said metallic cladding on said package core through one or more via connections.

11. The microelectronic device claimed in claim 1, wherein:

said die includes a plurality of power bars and a plurality of ground bars distributed on a surface thereof, each of said plurality of power bars being conductively coupled to multiple power bond pads of said die and each of said plurality of ground bars being conductively coupled to multiple ground bond pads of said die.

12. The microelectronic device claimed in claim 11, wherein:

said plurality of power bars and said plurality of ground bars are interleaved within a central region of said surface of said die.

13. The microelectronic device claimed in claim 11, wherein:

said die includes a plurality of signal contact pads distributed within a peripheral region of said surface.

14. The microelectronic device claimed in claim 1, wherein:

said metallization layer includes at least one power landing pad situated over said die, said at least one power landing pad being conductively coupled to multiple power bond pads on said die through corresponding via connections.

15. The microelectronic device claimed in claim 12, wherein:

said metallization layer includes at least one ground landing pad situated over said die, said at least one ground landing pad being conductively coupled to multiple ground bond pads on said die through corresponding via connections.

16. The microelectronic device claimed in claim 1, wherein:

said metallization layer includes at least one power landing pad situated over said package core, said at least one power landing pad being conductively coupled to multiple power bond pads on said die through a trace portion extending over said die and a plurality of via connections.

17. The microelectronic device claimed in claim 1, wherein:

said metallization layer includes at least one signal landing pad situated over said package core, said at least one signal landing pad being conductively coupled to a signal bond pad on said die through a path including a transmission line segment.

18. The microelectronic device claimed in claim 1, wherein:

said microelectronic device includes a single metallization layer between said die and said grid array interposer unit.

19. A method of fabricating a microelectronic device comprising:

fixing a die within an opening in a package core to create a die/core assembly;

applying a dielectric layer to a surface of said die/core assembly;

depositing a metallization layer above said dielectric layer, said metallization layer having a first metallization portion over said die and a second metallization portion over said package core;

providing a grid array interposer unit having a first surface and a second surface, said first surface having a metallization pattern for connection to said metallization layer of said die/core assembly and said second surface having an array of electrical contacts for connection to an external circuit board; and

laminating said grid array interposer unit to said die/core assembly so that said metallization pattern on said first surface thereof is conductively coupled to said metallization layer on said die/core assembly.

20. The method claimed in claim 19, comprising:

attaching at least one capacitor to said second surface of said grid array interposer unit to provide de-coupling for circuitry within said die.

21. The method claimed in claim 19, wherein:

said grid array interposer unit includes an opening that exposes a first portion of said metallization layer after said grid array interposer has been laminated to said die/core assembly, wherein said method comprises attaching a capacitor to said first portion of said metallization layer to provide de-coupling for circuitry within said die.

22. The method claimed in claim 19, wherein:

said array of electrical contacts includes a plurality of pins, said plurality of pins being attached to said grid array interposer unit before said grid array interposer unit is laminated to said die/core assembly.

23. The method claimed in claim 19, wherein:

depositing a metallization layer includes depositing at least one power landing pad and at least one ground landing pad over said die, said at least one power landing pad being conductively coupled to a plurality of power bond pads of said die and said at least one ground landing pad being conductively coupled to a plurality of ground bond pads on said die.

24. An electrical system comprising:

a microelectronic device having:

a die/core assembly including a die fixed within a package core, said die/core assembly having a first surface;

a metallization layer built up over said first surface of said die/core assembly, said metallization layer having a first metallization portion over said die and a second metallization portion over said package core; and

a grid array interposer unit laminated to said metallization layer, said grid array interposer unit having a first array of electrical contacts on a surface thereof; and

a circuit board having a second array of electrical contacts that correspond to said first array of electrical contacts on said grid array interposer unit, said grid array interposer unit being coupled to said circuit board so that each of said first array of electrical contacts is conductively coupled to a corresponding contact within said second array of electrical contacts.

25. The electrical system claimed in claim 24, wherein:

said circuit board is a computer motherboard.

26. The electrical system claimed in claim 24, wherein:

said first array of electrical contacts includes a plurality of pins.

27. The electrical system claimed in claim 24, wherein:

said first array of electrical contacts includes a plurality of solder balls.

28. A microelectronic device comprising:

a die/core assembly having a microelectronic die fixed within a package core, said die/core assembly including a first surface;

a metallization layer built up over said first surface of said die/core assembly, said metallization layer having a first metallization portion over said die and a second metallization portion over said package core;

a grid array interposer unit laminated to said metallization layer; and

at least one capacitor conductively coupled to an exposed portion of said metallization layer to provide de-coupling for circuitry within said microelectronic die.

29. The microelectronic device of claim 28, wherein:

said metallization layer includes at least one power landing pad situated over said microelectronic die that is conductively coupled to multiple power bond pads on said die and also to a corresponding power contact on said grid array interposer unit.

30. The microelectronic device of claim 28, wherein:

said metallization layer includes at least one power landing pad situated over said package core that is conductively coupled to multiple power bond pads on said die and also to a corresponding power contact on said grid array interposer unit.